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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Ulf ASSMUS et al.
Serial No. : 09/355,149
Filed : March 7, 2000
For : DEVICE AND METHOD FOR RECEIVING DATA
Art Unit : 2622
Examiner : Michael Lee
Confirmation No. : 6071

Commissioner for Patents
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Date: November 20, 2008

Signature: /Linda Lecomte/
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AMENDMENT

SIR:

In response to the Office Action made final dated May 20, 2008, please reconsider the above-identified application based on the following:

Amendments to the Claims are reflected in the listing of the claims which begins on page 2 of this paper.

Remarks begin on page 3 of this paper.

AMENDMENTS TO THE CLAIMS:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

LISTING OF CLAIMS:

1. (Previously Presented) A device for receiving data transmitted using asynchronous data transmission technology, a data-independent clock signal being added to the device, having a memory device, which stores the received data for the required period of time in order to compensate for transmission delays, characterized in that the clock signal is sent to the memory device for readout of the data.
2. (Previously Presented) The device according to claim 1, characterized in that it is designed for receiving data transmitted by the ATM technology.
3. (Previously Presented) The device according to claim 1, characterized in that the memory device is designed as a FIFO memory.
4. (Previously Presented) The device according to claim 3, characterized in that the FIFO memory is dimensioned so that the received data are storable for a period of preferably 100 Φ s to 250 Φ s per switching node.
5. (Previously Presented) The device according to claim 1, characterized in that a clock providing a clock signal is synchronized with at least one other device.
6. (Previously Presented) The device according to claim 1, characterized in that the clock is not synchronized with the clock of the transmitting device, and means for adjusting the received data stream to the clock rate of the clock are provided.
7. (Currently Amended) The device according to claim 6, characterized in that the clock rate adjusting means effect one of doubles and omits [[~~double or omit~~]] certain data signals when reading from the memory device.
8. (Previously Presented) The device according to claim 1, characterized in that the clock is synchronized via an external normal clock rate.
9. (Previously Presented) The device according to claim 1, characterized in that a switchover device is provided, which classifies the received data into data classes and relays them to a corresponding device.
10. to 17. (Canceled)

18. (Previously Presented) The device according to claim 1, wherein the asynchronous data transmission technology is at least one of audio data and video data.

REMARKS

Claim 7 has been amended to correct an informality. No new matter has been added. Claims 1 to 9 and 18 are now pending. Applicants respectfully request reconsideration of the present application in view of this response.

Claims 1 to 9 and 18 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,396,492 to Lien (“Lien reference”).

Applicants respectfully submit that the Lien reference does not identically describe or suggest each and every feature of the claims, as required for anticipation.

The Lien reference recites an adaptive clock recovery arrangement for deriving a synchronous clock from an asynchronous, packet stream such as an asynchronous transfer mode (ATM) cell stream. The Lien reference further recites that a deviation in the magnitude of information stored in a first-in-first-out memory is continually monitored, and the synchronous clock frequency, referred to as the adaptive line clock frequency, is adjusted in a plurality of modes, under the control of a processor. *According to the Lien reference, that adjustment is made in response to a detected increasing condition of the monitored deviation. The adjustments are open-loop adjustments made without continually adjusting the adaptive line clock frequency based on the monitored deviation.* The Lien reference refers to its differences from conventional PLL arrangements in that it includes a reduction in damping because the open-loop adjustments result in a rapid frequency correction with perfect or nearly perfect deadbeat damping, *i.e.*, without the frequency oscillations that continue after the correct frequency is reached in closed-loop arrangements.

Instead, claim 1 of the present invention concerns a device for receiving data transmitted using asynchronous data transmission technology. The device includes a data-independent clock signal and a memory device, and stores the received data for the required period of time in order to compensate for transmission delays. The clock signal is sent to the memory device for readout of the data. The Lien reference does not address this situation and instead focuses on the increasing condition of the monitored deviation, and effects a damping of the system. This is a different system than the one claimed in the present application. Accordingly, Applicants respectfully submit that claim 1 and its dependent claims 2 to 9 are allowable.

Claim 18 recites features analogous to claim 1, and is allowable for at least the same reasons as for claim 1. Accordingly, Applicants respectfully submit that claims 1 to 9 and 18 are allowable. Applicants respectfully request withdrawal of the rejection under 35 U.S.C. § 102(b) of those claims.

CONCLUSION

In view of the foregoing, it is believed that the rejection of the claims under 35 U.S.C. § 102(b) has been overcome, and that claims 1 to 9 and 18 are allowable. It is therefore respectfully requested that the rejections be withdrawn, and that the present application issue as early as possible.

In efforts to further the prosecution of this application, the undersigned would be happy to discuss the above application with the Examiner.

Respectfully submitted,

Dated: November 20, 2008

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